
































































04/19/01

U.S. UTILITY Patent Application

SCANNED  O.I.P.E.   O.A.

PATENT DATE

APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
09/836375	D	713	500	2182	Surajaram Lee

APPLICANTS

Peter Cook
Stanley Schuster

TITLE

Latch structure for interlocked pipelined CMOS (IPCMOS) circuits

PTO-2040
1289

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ISSUING CLASSIFICATION

ISSUING CLASSIFICATION												
ORIGINAL				CROSS REFERENCE(S)								
CLASS		SUBCLASS		CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)							
INTERNATIONAL CLASSIFICATION												

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<input type="checkbox"/> TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	_____ (Assistant Examiner) (Date)			NOTICE OF ALLOWANCE MAILED	
	_____ (Primary Examiner) (Date)			ISSUE FEE	
Amount Due				Date Paid	
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____ _____ _____	_____ (Primary Examiner) (Date)			ISSUE BATCH NUMBER	
				<input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.	
	_____ (Legal Instruments Examiner) (Date)				

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